CLAIMS

What is claimed is:

1. A method for transceiving data with a battery powered system, the method comprising the steps:

during a transmission period, operating a frequency agile device in accordance with data to be transmitted;

generating a modulated signal containing the data to be transmitted;

driving the modulated signal into a terminal of an IC, the terminal being associated with an IC voltage controlled oscillator (VCO) function, the VCO function being specified for operation within a first frequency range F1, and the modulated signal being within a second frequency range F2, where F2<F1;

generating a transmission signal from the modulated signal;

outputting the transmission signal from the IC and amplifying the transmission signal with an external amplifier prior to transmitting the transmission signal; and

during a reception period, receiving a signal.

2. A method as in claim 1 wherein the step of operating a frequency agile device further comprises the step of operating a direct digital synthesizer (DDS).

3. A method as in claim 1 wherein the step of generating a modulated signal further comprises the step of generating a frequency shift keying modulated signal.

4. A method as in claim 1 wherein the step of generating a modulated signal further comprises the step of generating a phase shift keying modulated signal.

5. A bimodal power data link transceiver device, the device comprising:

a transceiver integrated circuit (IC), the transceiver IC comprising:

a transmitter, the transmitter having;

a phase locked loop (PLL) frequency synthesizer;

a first power amplifier, the first power amplifier coupled to the PLL frequency synthesizer; and

a receiver;

a second power amplifier coupled to the first power amplifier;

a transmit/receive switch coupled to the second power amplifier and the receiver;

a controller coupled to the transceiver IC;

a direct digital frequency synthesizer having an output coupled to an input of the transceiver IC;

a second voltage controlled oscillator (VCO) coupled to the transmitter; and

a loop filter coupled to the second VCO and the transceiver IC.

6. A bimodal power data link transceiver device as in claim 5, wherein the PLL frequency synthesizer comprises:

a partial voltage controlled oscillator;

a phase detector coupled to the loop filter; and

a crystal oscillator coupled to the phase detector.

7. A bimodal power data link transceiver device as in claim 5, wherein the receiver comprises:

a low noise amplifier;

a quadrature mixer pair, the quadrature mixer pair coupled to the low noise amplifier and the PLL frequency synthesizer, the quadrature mixer pair having:

a first quadrature signal;

a second quadrature signal;

a demodulator;

a first signal channel, the first signal channel coupling the first quadrature signal to the demodulator; and

a second signal channel, the second signal channel coupling the second quadrature signal to the demodulator.

8. A bimodal power data link transceiver device as in claim 5, wherein the transceiver IC comprises at least one field programmable gate array (FPGA).

9. A bimodal power data link transceiver device as in claim 5 wherein the transmit/receive switch comprises a plurality of diodes.

10. A method for transceiving data in a device adapted to transceiving data in the radio frequency spectrum, the method comprising the steps of:

providing a transceiver integrated circuit (IC), the transceiver IC having:

an oscillator input port;

a frequency reference port;

a radio frequency input port;

a radio frequency output port;

a phase detector output port;

generating a voltage controlled oscillator (VCO) signal for input to the oscillator port;

coupling a direct digital synthesizer (DDS) to the frequency reference port;

coupling the radio frequency output port to a power amplifier;

coupling the radio frequency input port to a transmit/receive switch.

11. A method as in claim 10 wherein the step of providing a transceiver IC further comprises the steps of:

providing a field programmable gate array (FPGA);and

programming the FPGA to operate as a transceiver.

12. A method as in claim 10 wherein the step of generating a voltage controlled oscillator signal for input to the oscillator port further comprises the steps of;

coupling the phase detector output port to at least one loop filter; and

coupling the at least one loop filter to at least one VCO.

13. A method as in claim 10 wherein the step of coupling a DDS to the frequency reference port further comprises the step of coupling a first microprocessor controller to the DDS.

14. A method as in claim 13 wherein the step of coupling the first microprocessor controller to the DDS further comprises the step of setting a center transmit frequency.

15. A method as in claim 13 wherein the step of coupling the first microprocessor controller to the DDS further comprises the step of modulating a transmit frequency.

16. A method as in claim 10 wherein transceiving data in the device adapted to transceiving data in the radio frequency spectrum further comprises the steps of:

operating the device in a quiescent baseline receiver mode, wherein the quiescent baseline receiver mode comprises a first power mode;

operating the device in a burst transmit mode when not in the quiescent baseline receiver mode, wherein the burst transmit mode comprises a second power mode, wherein the second power mode is greater than the first power mode;

operating the device with a transmit/receive time ratio less than 1.5; and

transceiving a RF carrier frequency less than 200 MHz.

17. A method as in claim 10 wherein transceiving data in the device adapted to transceiving data in the radio frequency spectrum further comprises the step of operating the device with a global positioning indicator.

18. A method as in claim 10 wherein transceiving data in the device adapted to transceiving data further comprises the step of transceiving data in weapons munitions, wherein the step of transceiving data in weapons munitions further comprises the step of transmitting frequency shift key (FSK) modulated signals.

19. A method as in claim 10 wherein transceiving data in the device adapted to transceiving data further comprises the step of transceiving data in a landmine.

20. A bimodal power data link transceiver device, the device comprising:

a receiver section;

a transmitter section;

a phased locked loop (PLL) frequency generator section, wherein the PLL frequency generator section comprises:

a first voltage controlled oscillator (VCO);

an integrated circuit (IC), wherein the integrated circuit comprises:

a first buffer, wherein the buffer is coupled to the first VCO, the first buffer comprises:

a partial second VCO,

a digital direct synthesizer (DDS), wherein the DDS is coupled to the IC; and

a controller section, the controller section coupled to the PLL frequency generator section and the receiver section.

21. A bimodal power data link transceiver device as in claim 20, wherein the transmitter section comprises:

the IC, the IC further comprising:

a first amplifier, wherein the first amplifier is coupled to the PLL frequency generator section; and

a second amplifier, the second amplifier coupled to the first amplifier.

22. A bimodal power data link transceiver device as in claim 20, wherein the receiver section comprises:

a low noise amplifier;

a quadrature mixer pair coupled to the low noise amplifier; and

a demodulator coupled to the quadrature mixer pair.

23. A bimodal power data link transceiver device as in claim 20, wherein the device is adapted to fit in a weapon.

24. A bimodal power data link transceiver device as in claim 23 wherein the weapon comprises a landmine.

25. A bimodal power data link transceiver device as in claim 23 wherein the weapon comprises a sea mine.